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INTERUNIVERSITAIR MICRO-ELEKTRONICA CENTRUM [/]; (). WOUTERS, Dirk [/]; (). NORGA, Gerd [/]; (). NORGA, Gerd [/]; (). VAN MALDEREN, Joëlle ; ().

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(54) **Title: METHOD OF FABRICATION OF A FERRO-ELECTRIC CAPACITOR AND METHOD OF GROWING A PZT LAYER ON A SUBSTRATE**

(54) **Titre: PROCEDE DE FABRICATION D'UN CONDENSATEUR FERROELECTRIQUE ET PROCEDE DE FORMATION D'UNE COUCHE EN PZT SUR UN SUBSTRAT**

(57) Abstract

The present invention is related to a method, wherein a PZT layer (35) comprises a first PZT sub-layer and a second PZT sub-layer, the Ti-concentration of the first PZT sub-layer being higher than the Ti-concentration of the second PZT sub-layer.

(57) Abrégé

L'invention concerne un procédé, dans lequel une couche (35) en PZT comprend une première et une seconde sous-couches en PZT, la teneur en Ti de la première sous-couche étant supérieure à celle de la seconde sous-couche.

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(71) Applicants *(for all designated States except US)*: INTERUNIVERSITAIR MICRO–ELEKTRONICA CENTRUM [BE/BE]; Vereniging Zonder Winstbejag, Kapeldreef 75, B–3001 Heverlee (BE). WOUTERS, Dirk [BE/BE]; Burg. Frans Cnopslaan 2, B–3001 Leuven (BE).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: NORGA, Gerd [BE/BE]; Kleine Steenweg 59, B–2610 Antwerpen (BE).

(74) Agents: VAN MALDEREN, Joëlle et al.; Office Van Malderen, Place Reine Fabiola 6/1, B–1083 Brussels (BE).

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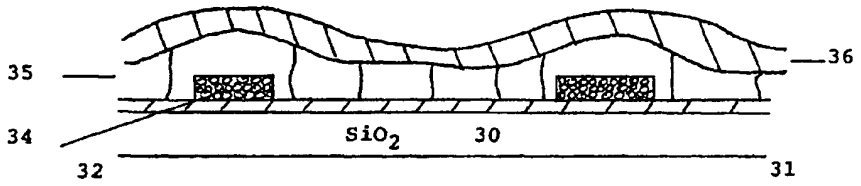

(57) Abstract

The present invention is related to a method, wherein a PZT layer (35) comprises a first PZT sub–layer and a second PZT sub–layer, the Ti–concentration of the first PZT sub–layer being higher than the Ti–concentration of the second PZT sub–layer.

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Description

METHOD OF FABRICATION OF A FERRO-ELECTRIC CAPACITOR AND METHOD OF GROWING A PZT LAYER ON A SUBSTRATE

Field of the invention

The present invention is related to a method of fabrication of a ferro-electric capacitor.

The present invention is also related to a method of growing a PZT layer on a substrate.

The present invention is also related to a ferro-electric capacitor.

The present invention is related to a 3D-capacitor.

Background of the present invention

There is a development in the art of non-volatile memories based on ferro-electric capacitors (FERAM-structure). In this development PZT films are an important candidate material. Such PZT films are ferro-electric layers comprising at least platinum, zirconium and titanium. Usually they are in the form of: $Pb(Zr, Ti) O_3$ or $(PbX) (Zr TiY) O_3$ where X= La and Y=Ta, are in small concentration as dopants.

A ferro-electric PZT based capacitor is formed by sandwiching a PZT layer between a first and a second electrode, the first electrode being a bottom electrode, the second electrode being a top electrode.

The principal advantage of PZT materials is their relatively low (500-600 °C) crystallisation temperatures which are compatible with a base line CMOS process and their high remanent polarisation.

As the deposition of a PZT layer directly on a bottom electrode such as a Pt-layer leads to poor fatigue performance of the capacitor, it was suggested to have a conductive oxide layer first deposited on the Pt-layer before the deposition of the PZT layer. This conductive oxide can be a unary oxide having a rutile crystal structure such as IrO_2, RuO_2 or OsO_2 or a complex oxide having a perovskite structure such as $(La,Sr)CoO_3$.

For the synthesis of ferroelectric PZT layers, use is often made of a two-step process:

- an amorphous layer is deposited, for instance by sol-gel or CVD or related techniques,
- this amorphous layer is converted into a ferro-electric layer having a perovskite crystal structure by a thermal treatment (crystallisation).

While the growth of oriented PZT layers is in principal facilitated by the use of perovskite electrodes, unary oxides are in practice preferred because they are readily synthesised by reactive sputtering. RuO_2 has received the most attention in this respect because of its relatively low resistivity (50 μΩcm, the lowest of the rutile type oxides), excellent diffusion barrier properties, and proven compatibility with silicon technology.

In order to obtain PZT ferro-electric layers showing high quality hysteresis loops and ferro-electric switching properties, it may be advantageous to achieve a strongly preferential (111) orientation of the grains making up the PZT layer.

This goal can be achieved by using a template layer having a (111) orientation such as a sputtered Pt layer with the (111) orientation.

In order to achieve the desired (111) orientation in the PZT layer, a conductive oxide is commonly grown under conditions so as to obtain a columnar microstructure on top of the so-called template layer which has the property that it can be deposited with a strongly preferred orientation. In this type of microstructure there is a fixed orientational relationship between the grains of the Pt layer and the grains of the conductive oxide layer.

So in other words such conductive oxide layer with a columnar microstructure can transmit the orientation of the underlying Pt layer to thereby assure that the PZT layer formed on this conductive oxide layer will have, after crystallisation, the same orientation as the underlying PT layer. Because the grains of the Pt are strongly preferentially (111) oriented, this means that the grains of the conductive oxide layer will be preferentially oriented as well. Because the grains of the PZT layer grown subsequently will again tend to have a fixed orientational relationship with the conductive oxide, it is possible in this way to grow highly oriented PZT layers having a (111) orientation.

However, this conventional approach described here above has several drawbacks.

Firstly, the need to make use of a template layer such as Pt represents a considerable process complication. However the template layer is needed because without it, the conductive oxide has the property to grow with random or mixed structure.

Secondly, the columnar structure of both the first layer, i.e. the template layer and the second layer, i.e. the conductive oxide layer leads to inferior diffusion

barrier properties of these layers. These diffusion barrier properties are necessary to protect the layers lying under the PZT layers against the indiffusion of oxygen during the growth of the PZT layer. This is of particular importance in a configuration where the bottom electrode of the capacitor is formed on a via connection, connecting said bottom electrode with the terminal of an active device, e.g. a MOSFET. This out-diffusion of oxygen can lead to a degradation of the electrical properties, particularly the conductivity, of this via connection.

Thirdly, the growth of a PZT layer on a bottom electrode with a columnar structure can have, depending on the application, a further disadvantage as it leads to PZT layers with small grain sizes, typically 100 to 200 nm lateral dimension. This small grain size is the result of the high nucleation rate of PZT on columnar layers during the crystallisation treatment. This high nucleation rate is due to the large surface roughness of columnar layers. This surface roughness is caused by the grains of the conductive oxide, which have the tendency to form facets. These facets form fixed angles with respect to the growth direction. Due to this effect, layers with smaller grains have a lower surface roughness. A higher surface roughness makes the formation of a nucleus with the desired crystal structure energetically favourable during crystallisation because the nucleation can take place in a recess at the surface between two adjacent grains thereby minimising the required amount of surface that needs to be created for formation of the nucleus. The small grained PZT layers obtained on columnar electrode layers renders the fabrication of ferro-electric devices on a single PZT grain impossible. Ferro-electric capacitors comprising a PZT layer being composed of a single grain are known to exhibit superior properties such as abrupt ferro-electric

switching, low leakage current and high endurance compared to capacitors comprising multiple grains as such multiple grain capacitors incorporate grain boundaries.

Fourthly, fabrication of 3D capacitors using a columnar bottom electrode leads to an undesirable orientation of the PZT grown on the sidewalls. This misorientation implies that the purpose of 3D-capacitor fabrication, namely a gain in the amount of switchable charge per unit area on the wafer, is defeated. To avoid this problem, a new method has to be developed which does not employ the orientation of the bottom electrode grains as a means to control the orientation of the PZT grains.

Aims of the invention

The present invention aims to suggest a method of growing a PZT layer on a bottom electrode and accordingly a method of fabrication of a ferro-electric capacitor which do not have the drawbacks of the state of the art.

Main characteristics of the present invention

According to a first aspect, the present invention is related to a method of fabricating a ferro-electric capacitor comprising the steps of:

- creating a first electrode consisting essentially in a layer of a conductive oxide on a substrate,
- forming a ferro-electric PZT layer on said conductive oxide layer,
- creating a second electrode isolated from said first electrode on the top of the ferro-electric PZT layer,
- wherein said conductive oxide layer comprises at least two sub-layers of individual grains, the top sub-layer having a random orientation of the individual grains.

Said conductive layer has a micro- or nano-crystalline structure. Preferably the conductive oxide layer has a grain size at least two times and preferably five times smaller than the conductive oxide layer thickness.

According to a first preferred embodiment said conductive layer is made of a unary oxide, preferably having a rutile crystal structure such as IrO_2, RuO_2, RhO_2, ReO_2 or OsO_2.

According to another preferred embodiment said conductive layer is made of a complex oxide having a perovskite crystal structure such as $(La,Sr)CoO_3$.

According to a preferred embodiment said PZT layer comprises a first PZT sub-layer and a second PZT sub-layer, the Ti-concentration of the first PZT sub-layer being higher than the Ti-concentration of the second PZT sub-layer.

The step of creating a ferro-electric PZT layer consists in:

- deposition of an amorphous PZT layer,
- crystallisation of said amorphous layer into a ferro-electric PZT layer by a thermal treatment.

Advantageously, said PZT-layer will have a (111)-orientation.

According to a preferred embodiment the method further comprises, before creating the first electrode, the steps of:

- depositing a contact layer on an active device,
- depositing a conductive via connection on said contact layer.

Said active device can be a MOSFET.

According to a second aspect, the present invention is related to a method of growing a PZT layer

directly on a conductive oxide layer formed on a substrate, wherein said conductive layer comprises at least two sub-layers of individual grains, the top sub-layer having a random orientation of individual grains.

During the growing of the conductive oxide layer, said substrate has a temperature comprised between a first predetermined temperature Tc1 and a second predetermined temperature Tc2, Tc1 being defined by the temperature below which the sub-layers of the conductive oxide layer being amorphous, Tc2 being defined by the temperature which ensures that the grain size of the conductive oxide layer does not exceed a predetermined dimension, preferably of the order of several nanometers and typically of the order of 20nm.

The atmosphere during the growing of the PZT layer is preferably a O_2/Ar mixing atmosphere having a ratio above 1 and preferably above 4/1.

The deposition rate during the growing of the conductive oxide layer is comprised in the range 15-20 nm/min.

Preferably said conductive oxide layer has a grain size at least two times and preferably five times smaller than the PZT layer thickness.

As a third aspect, the present invention is related to a ferro-electric capacitor comprising at least:

- a first electrode,
- a second electrode being isolated from said first electrode,
- a ferro-electric PZT layer being sandwiched between said first electrode and said second electrode,

wherein said first electrode comprises at least a layer of a conductive oxide having at least two sub-layers of individual grains, the top sub-layer showing a random

orientation of individual grains and a nano-crystalline structure, with preferably a grain size <20 nm.

According to a first preferred embodiment said conductive layer is made of a unary oxide, preferably having a rutile crystal structure such as IrO_2, RuO_2, RhO_2, ReO_2 or O_sO_2.

According to another preferred embodiment said conductive layer is made of a complex oxide having a perovskite crystal structure such as $(La,Sr)CoO_3$.

Advantageously, said conductive oxide layer will have a (111) orientation.

According to a preferred embodiment said PZT layer comprises a first PZT sub-layer and a second PZT sub-layer, the Ti-concentration of the first PZT sub-layer being higher than the Ti-concentration of the second PZT sub-layer.

According to a fourth aspect, the present invention is related to a 3-dimensional ferro-electric capacitor comprising

- a first electrode,
- a second electrode being isolated from said first electrode,
- a ferro-electric PZT layer being sandwiched between said first electrode and said second electrode wherein said PZT layer has the form of one horizontal surface and two sidewalls overlapping said first electrode,

wherein said first electrode comprises at least a layer of a conductive oxide having at least two sub-layers of individual grains, the top sub-layer showing a random orientation of individual grains, preferably with a grain size <20 nm.

Short description of the drawings

Figure 1 is representing a method for growing a (111) orientated PZT layer on an arbitrary substrate according to the state of the art.

Figure 2 is describing a method of growing a (111) orientated PZT layer on an arbitrary substrate according to the present invention.

Figure 3 is representing the effect of a bottom electrode in the present case made of RuO_2 growth temperature on the texture of the PZT layer.

Figure 4a and 4b are representing the hysteresis measurements for a capacitor having a RuO_2 bottom electrode layer, grown at 350°C wherein figure 5a is showing the nested loops from 1 to 7 V with 1 V steps and figure 5b is representing the remanent polarisation (P_r) and saturation polarisation (P_{sat}) versus the voltage.

Figure 5a and 5b are representing the hysteresis measurements for a capacitor having a RuO_2 bottom electrode layer, grown at 150°C wherein figure 6a is showing the nested loops from 1 to 7 V with 1 V steps and figure 5b is representing the remanent polarisation (P_r) and saturation polarisation (P_{sat}) versus the voltage.

Figure 6 is representing the pulse switching results for a sample with a RuO_2 bottom electrode layer, grown at 150 and 200 °C.

Figure 7 is representing the fatigue result for a sample with RuO_2 bottom electrode layer, grown at 150 and 200 °C.

Figure 8 is representing several embodiments of a ferro-electric capacitor fabricated according to the method of the present invention.

Figure 9 is representing a 3D-capacitor fabricated according to the present invention.

Detailed description of several embodiments of the present invention

The present invention will be described more in detail with reference to the several drawings wherein:

Figure 1 is representing a method for growing a (111) oriented PZT layer on an arbitrary substrate for instance SiO_2 according to the state of the art. On said SiO_2 substrate (11), a template layer (13) such as a Pt layer is deposited with an adhesion layer (12) there between. Thereafter a conductive oxide layer (14) such as RuO_2 is deposited. Said Pt layer (13) has a (111) orientation. Because the grains of the Pt layer (13) are strongly preferentially (111) orientated, the grains of the conductive oxide layer (14) deposited thereon are also preferentially oriented.

The grains of the PZT layer (15) grown subsequently on the conductive oxide layer (14) will also tend to have said preferentially (111) orientation even in the case that the said conductive oxide layer (14) present a preferential (100) orientation. The grains of the PZT layer (15) grown subsequently on said conductive oxide layer (14) will also tend to have the preferential (111) orientation.

Figure 2 is representing a method for growing a strongly (111) oriented PZT layer (25) on a conductive oxide layer (24) without the need of a template layer. As represented in said figure, a nano-crystalline conductive oxide layer (24), preferably of the rutile or perovskite structure, which has a grain size of less than 20 nm is used.

The synthesis of PZT films with the desired nano-crystalline microstructure is possible by choosing a specific combination of deposition variables, namely the

substrate temperature, the deposition rate, and the Oxygen/Argon mixing ratio in the case of reactive sputtering.

(1) When using sputter deposition with a metallic target, a sufficiently high Oxygen/Argon mixing ratio is needed to ensure full oxidation of the target material,

(2) The substrate temperature should be above a minimum temperature Tc1 being defined when the conductive oxide layer is still amorphous. Such amorphous conductive oxide layers are not desired because of their poor stability in ambient air.

(3) The substrate temperature should be low enough (below a critical temperature Tc2) to ensure that the (lateral) grain size of the individual grains does not exceed 20nm. Above this temperature the enhanced surface diffusivity results in films with coarser grains.

(4) The deposition rate should be sufficiently high (above a critical deposition rate r_c) to ensure that a film with a granular rather than a columnar microstructure is formed. Above r_c, the arrival rate of sputtered atoms is high enough to ensure nucleation of new grains on top of existing rains during growth of the layer. Because of increasing surface diffusivity, rc increases as the deposition temperature is increased (for the same material).

Because the temperature T_{c1} and T_{c2} scale with the absolute melting temperature, T_m, of the metal atoms being sputtered, the specific process window following from the above requirements will vary depending on the type of conductive oxide. Furthermore, T_{c1} and T_{e2} will generally be higher for complex (binary or ternary) oxides with the perovskite structure such as $(La,Sr)CoO_3$ than for unary

oxides such as the rutile-structure oxides such as RuO_2, IrO_2, RhO_2, OsO_2, ReO_2,...

For instance, for the case of RuO_2 prepared by reactive sputtering, films with the desired nanocrystalline structure can be prepared using substrate temperatures in the range 100-150C and corresponding deposition rates r_c=15-20 nm/min. When using a metallic Ru target, an O_2/Ar mixing ration of 4/1 is needed to ensure full oxidation of Ru to RuO_2.

Processing windows for other materials can be calculated based on their absolute melting temperature. For instance, for Osmium (Os), $T_m(Os)=330°K=1.3xT_m(Ru)$, and hence the deposition window is 215°C-275°C for Os, for the same deposition rates.

No fixed orientational relationship exists between the grains of the conductive oxide layer and the grains of the underlying layer (if this underlying layer has at all a preferential orientation). Due to the absence of a preferential orientation in the grains making up the surface of the layer, orientation selection in a PZT layer grown on top of this nano-crystalline conductive oxide layer will occur in a fashion which is distinct from the case of a conductive oxide layer with columnar structure. Instead of growing with a fixed orientational relationship with respect to the grains on which it grows, the PZT will grow with an orientation which minimises the surface energy needed to create a nucleus of crystallisation. For PZT, the orientation corresponding to minimal surface energy is the (111) orientation. For this reason, the orientation of a PZT layer grown on a nano-crystalline or granular conductive oxide layer will be (111), without the need for a preferential orientation in the grains making up the top layer of the conductive oxide layer and without the need of a template layer. The thermal treatments required for the

crystallisation of the PZT layer hardly affect the nano-crystalline structure of the conductive oxide layers.

Since the grains of a nano-crystalline conductive oxide layer are typically 20 nm or smaller, this means several times smaller than the grain size in a columnar layer, the roughness of the granular layer is accordingly smaller than the roughness of the columnar layer. Because of the lower surface roughness of the nano-crystalline conductive oxide, the rate of formation of nuclei of PZT of the desired rutile or perovskite phase will be lower than on the columnar layer. Because the growth rate of the nuclei will not be affected by changes in the roughness of the layers, this will lead to a larger grain size (typically 10 to 100 times larger) in case of a nano-crystalline conductive oxide bottom electrode layer.

Figure 3 shows the effect of bottom electrode growth temperature on the texture of the PZT grown on top. For high growth temperatures, where the RuO_2 layer has columnar structure, the PZT texture is mixed (111)/(101)/(100). This mixed PZT texture results from a mixed texture of the RuO_2. This mixed texture results because of the random texture of the RuO_2 layer grown on Pt. As the temperature of the substrate during bottom electrode sputtering is reduced, the grain size of the RuO_2 film becomes smaller (which is reflected in the decreasing intensity of the RuO_2 (110) peak), and the PZT becomes preferentially (111). The temperature at which the transition to a strongly (111) oriented layer occurs is between 250 and 150 ^{o}C; this is also the transition region between RuO_2 with columnar and granular structure. However, the value of this critical temperature where the desired transition from columnar to granular conductive oxide material, and hence also from mixed oriented to sharply

(111) oriented PZT occurs, may depend considerably on the particular bottom electrode material, on process variables such as the deposition rate, and on the type of layer on which the conductive oxide is grown.

An example of the effect of bottom electrode grain structure on the properties of a ferro-electric capacitor device is shown in Figure 4 and 5. Shown in Figure 4 is the hysteresis characteristic for a randomly textured RuO_2 bottom electrode with columnar structure. The bottom electrode was grown at 350 ^oC. The hysteresis loop is slanted, i.e. the slope at the intersection point with the field axis is relatively small. This is indicative of slow switching behaviour which makes the material less suitable for memory circuit applications. The slanting in the loop is due to a mixed texture in the PZT for this growth temperature of the bottom electrode layer.

Shown in Figure 5 is the hysteresis loop for a RuO_2/PZT/RuO_2 FECAP where the RuO_2 bottom electrode was grown at a low temperature (150°C) resulting in a granular RuO_2 structure.

Figure 6 compares the pulse switching behaviour for a sample with RuO_2 grown at 150 and a sample grown at 200 ^oC. The excellent pulse switching behaviour of the sample with the RuO_2 grown at the lowest temperature demonstrates the effect of texture on pulse switching behaviour. Referring back to Figure 3, we conclude that a very sharp (111) PZT texture ((111)/((101) +(100)) > 100) is necessary to achieve good pulse switching results.

Figure 7 demonstrates that the same requirement applies for obtaining optimal fatigue performance of the layers.

These results illustrate the overall improvement in ferro-electric properties, resulting from a

highly preferential (111) texture, which can be achieved by using a bottom electrode with a granular structure.

An exemplary embodiment of a ferro-electric capacitor based on the principle described in figure 2, is shown in Figure 8a and 8b.

In figure 8a is represented a ferro-electric capacitor formed by sandwiching a PZT layer (35) between a first and a second electrode, the first electrode being the bottom electrode (34), the second electrode being the top electrode (36).

According to the present invention, said first electrode (34) is made of a conductive oxide layer having a nano-crystalline structure and comprising at least two sub-layers of individual grains, wherein the top-layer has a random orientation of the individual grains. Said conductive oxide layer can be a unary oxide, e.g. IrO_2, RuO_2, RhO_2, ReO_2, OsO_2 or can be a complex oxide, e.g. $(La,Sr)CoO_3$.

The use of a nano-crystalline conductive oxide layer obviates the need for a template layer with a preferential orientation, such as a Pt layer with the (111) orientation, for the achievement of a preferential (111) orientation in the PZT layer.

This means that a conductive oxide bottom electrode (34) layer with a nano-crystalline structure can be deposited on any arbitrary other underlying layer such as an optional barrier layer (31), without any requirement towards orientation, while still maintaining the desired (111) orientation in the PZT layer (35), grown on top of the conductive oxide layer (34). Thus the new bottom electrode concept leads to less complexity in the processing and more flexibility in the choice of layers forming the bottom electrode stack.

Particularly, in the case as represented in Figure 8c where a direct contact has to be established between the bottom electrode (34) and a Si substrate or a via connection (38), the new bottom electrode concept is useful because it facilitates the development of the stack of materials which is required to establish a reliable electrical connection between an active device made in the underlying semiconductor substrate and the conductive oxide layer (34), which serves as bottom electrode layer of the ferro-electric capacitor.

Preferably, a conductive via connection (38) connecting said bottom electrode (34) to an electrode or contact layer (39) of an active device (40) is suggested, said device being formed in an underlying semiconductor substrate. Particularly said conductive via connection (39) can be a metal like e.g. Al, Cu, W or an alloy of ans of these materials or even a Poly Si plug. An example of such an active device (40) is a MOSFET.

More precisely, the nano-crystalline conductive oxide layer (34) can be deposited on top of a metal barrier layer (31), e.g. Ir, Ru, Rh, Re, Os which forms a conductive oxide upon oxidation, without any texture requirement for this metal barrier layer. Said metal barrier layer (31) is on its turn deposited on the via connection. Due to the excellent diffusion barrier properties of the nano-crystalline conductive oxide layer, the crystallisation treatment of the PZT formed thereon will not lead to any oxidation or decrease in conductance of the via connection material.

Other diffusion barrier layers can also be used such as Ta- or Ti-based barrier layers, e.g. TaN or TiN, or other Ta- or Ti-based barrier layers such as TiAlN or TaSiN.

According to a preferred embodiment, the PZT layer can comprise at least a first PZT sub-layer and a second PZT sub-layer on said first sub-layer, said first sub-layer being adjacent to the bottom electrode and having a Ti concentration being higher than the Ti concentration in said second sub-layer.

Growth of highly (111) oriented PZT layers can be performed for example by the sol-gel, sputter or CVD deposition techniques. For PZT layers with a Zr/(Zr+Ti) concentration larger than 0.2, crystallinity of the layers formed can be improved by first depositing a thin seedlayer of high Ti PZT. Particularly, seedlayers having a Zr/(Zr+Ti) smaller than 0.2 are formed. Doing so reduces the reactivity of lead or lead oxide, which is not yet incorporated in the PZT layer, towards the underlying electrode layer. This lead or lead oxide would otherwise react with the bottom electrode to form conducting compounds which increase the leakage current of the ferro-electric device. By using the high-Ti PZT seedlayer, ferro-electric layers can be obtained which are single phase perovskite and (111) oriented, featuring abrupt ferro-electric switching, high remnant polarisation and low fatigue rate.

The possibility to grow layers with significantly larger grains than with conventional methods is useful because it allows the fabrication of ferro-electric devices, e.g. ferro-electric capacitors for non-volatile memories, on a single PZT grain or crystal. Such devices have been shown to exhibit superior switching quality, endurance and leakage current compared to devices fabricated on more than one grain as such devices incorporate at least one grain boundary.

The fabrication schemes contained in the respective embodiments are of particular importance in

light of the current technological evolution in PZT-based non-volatile memories. In figure 9 the evolution in cell layout with increasing circuit density is sketched. In the case of the low density, planar cell layout (Fig 9a), the use of a template layer, such as Pt, to induce the required orientation in the PZT does not result in added process complexity. Meanwhile, in the case of the planar stacked cell, Fig 9b, which is required for medium density circuits, the bottom electrode should also serve as diffusion barrier to prevent oxidation of the plug material (resulting in loss of its conductive properties) during crystallisation of the ferro-electric. For this purpose, Pt is not suited because of its poor diffusion barrier properties for oxygen. Template layers, used to induce the required orientation in the PZT, represent a process complication while not necessarily improving the barrier properties of the stack. For this case, the proposed fabrication scheme, employing a nano-crystalline or granular bottom electrode, provides a solution requiring a minimum number of layers, at the same time ensuring that the desired texture in the ferro-electric is achieved and effectively preventing oxygen from reaching the plug material. Hence the granular conductive oxide can be grown on top of the plug material (or alternately a supplemental barrier layer may be interposed). Its granular structure guarantees that the desired (111) PZT texture is obtained without the need to control the texture in the plug material/barrier layer/bottom electrode stack.

For circuit densities of 1Gb and greater, stacked cell layouts with 3D capacitors (Fig 9c) are necessary, because the need to maintain adequate signal intensity during read-out of the cell implies that the remanent polarisation per unit area has to be increased. Three dimensional capacitors are only effective if the

ferro-electric maintains the desired orientation with respect to the electrical field lines both on the horizontal electrode surface and electrode sidewalls. Because the field lines run approximately normal to the electrode surface, this implies that the ferro-electric should maintain a fixed orientation with respect to the surface normal on both the horizontal electrode surface and the electrode sidewalls. Since for a columnar electrode, the crystal facets exposed on the sidewall and top surface are necessarily different, this type of electrode structure would inevitably lead to non-optimal orientation and hence low signal contribution from either the top surface or the sidewalls. Meanwhile, the use of a granular bottom electrode will guarantee that the same orientation between the ferro-electric and the electrode surface is maintained at all times. By using this approach, the aim of the 3D capacitor, namely to increase signal strength/unit area, can be fully achieved.

Best mode

Silicon wafers with a thermal oxide layer are used as substrate for the growth of ferro-electric capacitor (FECAP) structures. After deposition of 10 nm Ti followed by 150 nm Pt by Rf sputtering, the wafers are annealed by rapid thermal processing (RTA) at 700°C for 5 min. to stabilize the reactive PT/Ti stack. Subsequent RuO_2 deposition is performed by reactive DC sputtering in an O_2/Ar mixture. To prevent the deposition of partially oxidized films which are not stable during later thermal process steps, a low sputter power (100W) and an oxygen rich sputter ambient (80% O_2 in Ar) are employed. Gas flows are adjusted so that a gas pressure of $8x10^{-3}$ mbar is obtained prior to sputtering. Substrate temperatures for bottom electrode sputtering are varied between 150 and

350°C. The samples are placed on a ceramic support wafer, which is heated from below with a radiative heating element. The temperature is controlled using a thermocouple positioned close to the bottom side of the support wafer.

Thin films of ferro-electric $Pb(Zr,Ti)O_3$ are deposited by spin coating of an alkoxide-type sol-gel precursor using buthoxyethanol as solvent. To compensate for Pb evaporation during thermal treatment, a Pb excess of 15% with respect to the stoichiometric amount is added. Four sub-layers, each approximately 65 nm thick are deposited, with separate drying and pyrolysis steps carried out after each layer on temperature controlled hot plates. Drying is performed at 200°C for 2 min., pyrolysis at 400°C for 2 min. To increase the nucleation rate and improve the crystallinity of the layers a lower Zr/Ti concentration (20/80) is used for the first sub-layer than for the next three sub-layers (Zr/Ri+30/70). Finally, the layers are crystallised by RTA for 5 min. at 700°C in O_2. A 20°C/s ramp rate was used.

RuO_2 top electrodes are deposited by reactive sputtering, using the same pressure and Ar/O_2 mixing ratio as used for the bottom electrode sputtering process. No intentional substrate heating is used during the deposition of the top electrodes. Large area (0.0028 cm^2) top electrodes were deposited using a shadow mask while smaller size (2000 m^2) capacitors were patterned using conventional photoresist photolithography and dry etching.

Claims

CLAIMS

1. Method of fabricating a ferro-electric capacitor comprising the steps of:

- creating a first electrode consisting essentially in a layer of a conductive oxide (34) on a substrate (30),
- forming a ferro-electric PZT layer (35) on said conductive oxide layer (34),
- creating a second electrode (36) isolated from said first electrode on the top of the ferro-electric PZT layer (35),

wherein said conductive oxide layer (34) comprises at least two sub-layers (341 and 342) of individual grains, the top sub-layer (342) having a random orientation of individual grains.

2. Method according to claim 1 wherein said conductive oxide layer (34) has a micro- or a nano-crystalline structure.

3. Method according to claim 1 or 2, wherein said conductive oxide layer (34) has a grain size which is at most 50 nm.

4. Method according to claim 3, wherein the grain size of the conductive oxide layer (34) is at most 20 nm.

5. Method according to any one of the preceding claims wherein said conductive oxide layer (34) is made of a unary oxide, preferably having a rutile crystal structure such as IrO_2, RuO_2, RhO_2, ReO_2 or OsO_2.

6. Method according to any one of the preceding claims wherein said conductive oxide layer (34) is made of a complex oxide having a perovskite crystal structure such as $(La,Sr)CoO_3$.

7. Method according to any one of the preceding claims, wherein said PZT layer (35) comprises a first PZT sub-layer and a second PZT sub-layer, the Ti-concentration of the first PZT sub-layer being higher than the Ti-concentration of the second PZT sub-layer.

8. Method according to anyone of the preceding claims wherein the step of forming a ferro-electric PZT layer consists in:

- deposition of an amorphous PZT layer,
- crystallisation of said amorphous layer into a ferro-electric PZT layer by a thermal treatment.

9. Method according to any one of the preceding claims, wherein said PZT layer (35) has a (111)-orientation.

10. Method according to any one of the preceding claims, further comprising, before creating the first electrode (34), the steps of:

- depositing a contact layer (39) on an active device (40),
- depositing a conductive via connection (38) on said contact layer (39).

11. Method according to claim 10, characterised in that said active device (40) is a MOSFET.

12. Method of growing a PZT layer directly on a conductive oxide layer formed on a substrate wherein said oxide layer comprises at least two sub-layers of individual grains, the top sub-layer having a random orientation of individual grains.

13. Method according to claim 12 wherein the temperature of the substrate during the growing of the PZT layer is comprised between a first predetermined temperature Tc1 and a second predetermined temperature Tc2, Tc1 being defined by the temperature below which the sub-

layers of the conductive oxide layer being amorphous, Tc2 being defined by the temperature which ensures that the grain size of the PZT layer does not exceed a predetermined dimension preferably of the order of 20 nm.

14. Method according to claim 12 or 13, wherein the atmosphere during the growing of the PZT layer is a O_2/Ar mixing atmosphere having a ratio above 1 and preferably above 4/1.

15. Method according to any one of the preceding claims 12 to 14, wherein the deposition rate of the PZT layer during the growth is comprised in a range 15-20 nm/min.

16. Method according to any one of the preceding claims 12 to 15, wherein said conductive oxide layer has a grain size at least two times and preferably five times smaller than the PZT layer thickness.

17. A ferro-electric capacitor comprising:

- a first electrode (34),
- a second electrode (36) being isolated from said first electrode (34),
- a ferro-electric PZT layer (35) being sandwiched between said first electrode (34) and said second electrode (36),

wherein said first electrode (34) comprises at least a layer of a conductive oxide having at least two sub-layers of individual grains, the top sub-layer having a random orientation of individual grains.

18. A ferro-electric capacitor according to claim 17 wherein said conductive layer has a micro- or an a nano-crystalline structure.

19. A ferro-electric capacitor according to claim 18 wherein said conductive oxide layer (34) has a grain size which is at most 50 nm.

20. A ferro-electric capacitor according to claim 19 wherein the grain size of said conductive oxide layer (34) is at most 20 nm.

21. A ferro-electric capacitor according to any one of the preceding claims 17-20 wherein said conductive oxide layer (34) is made of a unary oxide, preferably having a rutile crystal structure such as IrO_2, RuO_2, RhO_2, ReO_2 or OsO_2.

22. A ferro-electric capacitor according to any one of the preceding claims 17-21 wherein said conductive oxide layer (34) is made of a complex oxide having a perovskite crystal layer such as $(La,Sr)CoO_3$.

23. A ferro-electric capacitor according to any one of the preceding claims 17-22 wherein said PZT layer (35) has a (111)-orientation.

24. Capacitor according to any one of the claims 17-23, being connected to an electrode (39) of an active device (40) through a via connection (38).

25. A ferro-electric capacitor comprising

- a first electrode (44),
- a second electrode (46) being isolated from said first electrode (44),
- a ferro-electric PZT layer (45) being sandwiched between said first electrode (44) and said second electrode (46) wherein said PZT layer (45) has the form of one horizontal surface with sidewalls overlapping said first electrode (44),

wherein said first electrode (34) comprises at least a layer of a conductive oxide having at least two sub-layers of individual grains, the top sub-layer having a random orientation of individual grains.

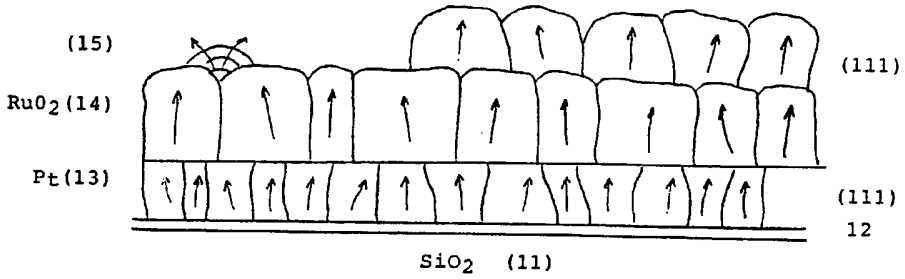
(15)
RuO_2 (14)
Pt(13)
(111)
(111)
12
SiO_2 (11)

Fig. 1

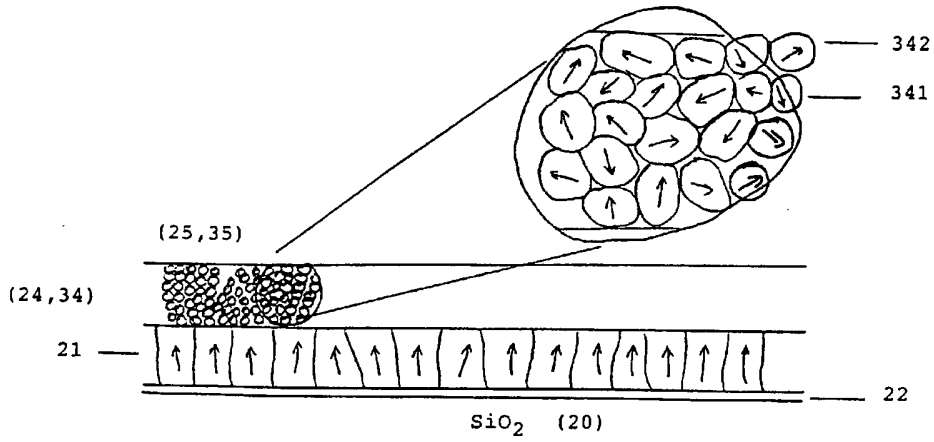
342
341
(25,35)
(24,34)
21
22
SiO_2 (20)

Fig. 2

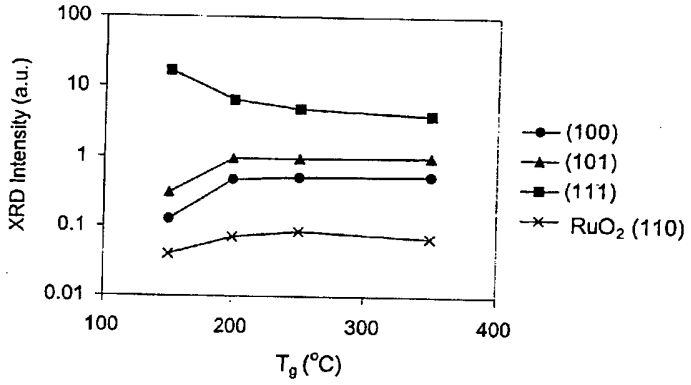
100
10
1
0.1
0.01
XRD Intensity (a.u.)
100
200
300
400
T_g (°C)
(100)
(101)
(111)
RuO_2 (110)

Fig. 3

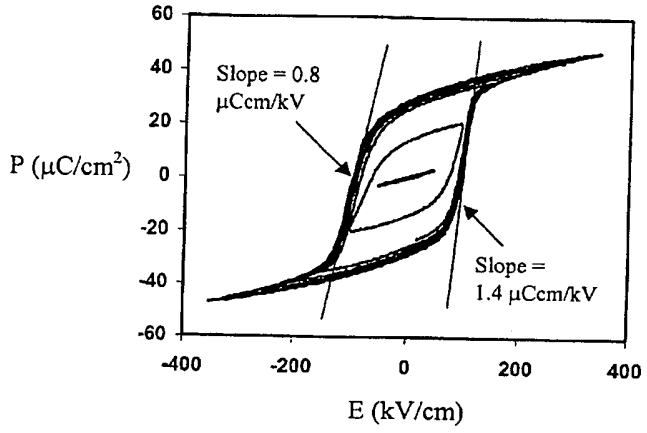
60
40
20
0
-20
-40
-60
-400
-200
0
200
400
P (μC/cm²)
E (kV/cm)
Slope = 0.8
μCcm/kV
Slope =
1.4 μCcm/kV

Fig. 4 a

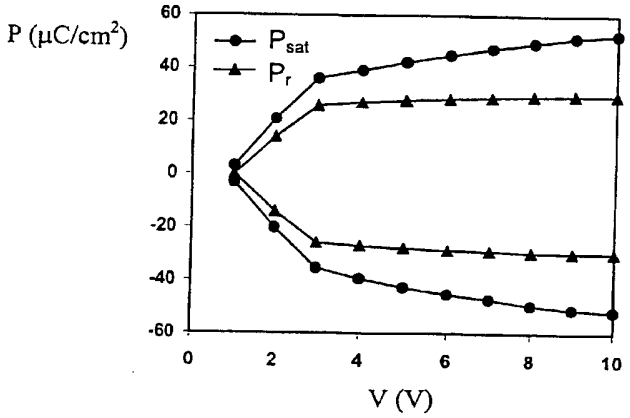
60
40
20
0
-20
-40
-60
0
2
4
6
8
10
P (μC/cm²)
V (V)
Psat
Pr

Fig. 4 b

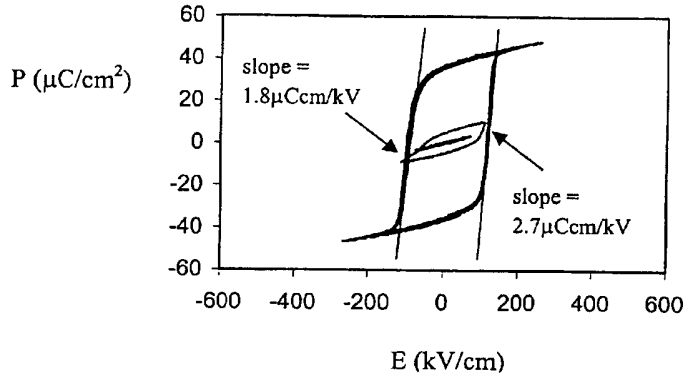
P (μC/cm²)
60
40
20
0
-20
-40
-60
slope =
1.8μCcm/kV
slope =
2.7μCcm/kV
-600
-400
-200
0
200
400
600
E (kV/cm)

Fig. 5 a

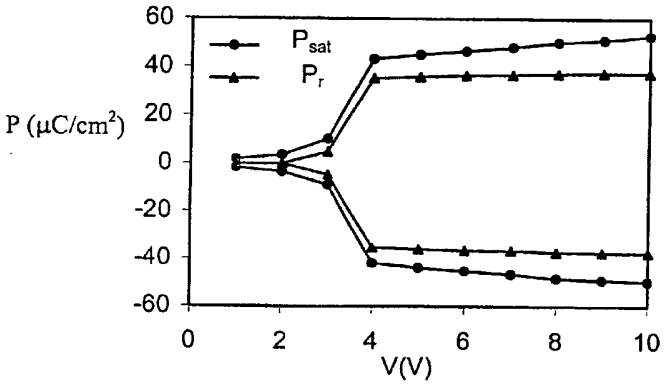
P (μC/cm²)
60
40
20
0
-20
-40
-60
Psat
Pr
0
2
4
6
8
10
V(V)

Fig. 5 b

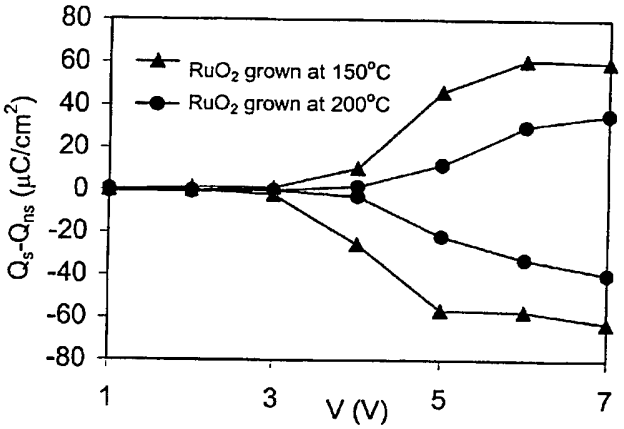
80
60
40
20
0
-20
-40
-60
-80
1
3
5
7
V (V)
Q_s-Q_{ns} (μC/cm^2)
RuO_2 grown at 150°C
RuO_2 grown at 200°C

Fig. 6

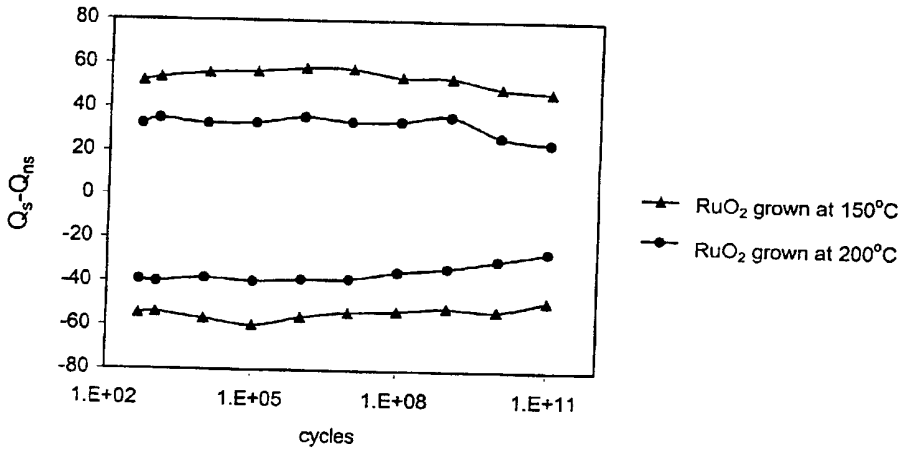
80
60
40
20
0
-20
-40
-60
-80
Q_s-Q_{ns}
1.E+02
1.E+05
1.E+08
1.E+11
cycles
RuO_2 grown at 150°C
RuO_2 grown at 200°C

Fig. 7

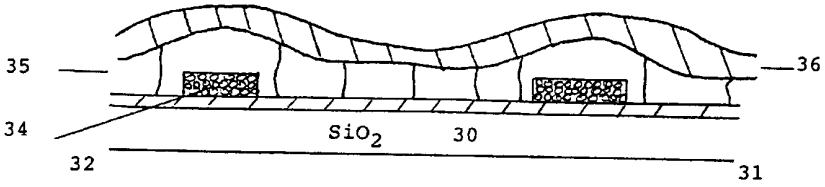

Fig. 8a

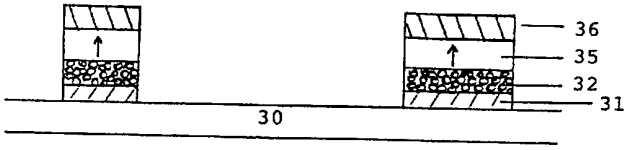

Fig. 8b

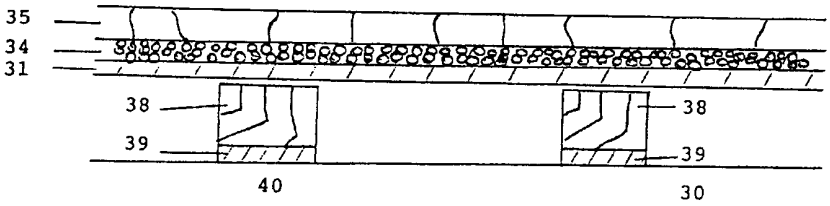

Fig. 8c

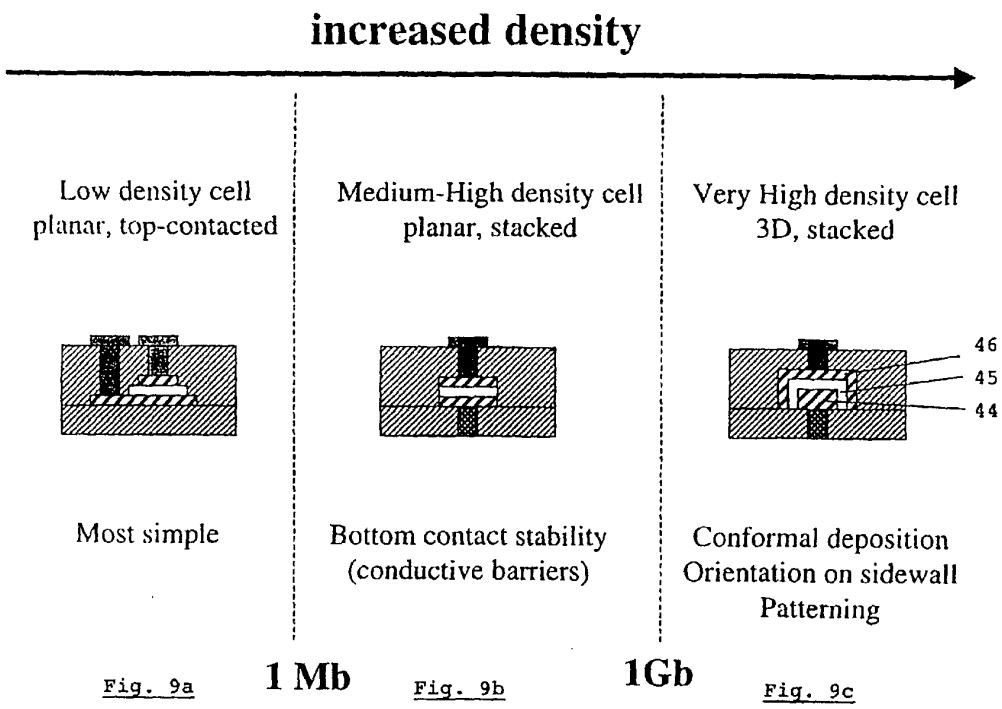

Fig. 9a Fig. 9b Fig. 9c

INTERNATIONAL SEARCH REPORT

Internatio \pplication No
PCT/BE 99/00155

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	MCINTYRE D S, SAYER M, WEAVER L, GRISWOLD E M, CHIVUKULA V: "Electrical characterization of PZT on rapid thermally annealed ruthenium oxide electrodes" INTEGRATED FERROELECTRICS, 1995, GORDON & BREACH, UK,1995, pages 301-308, XP000884827 Seventh International Symposium on Integrated Ferroelectrics, Colorado Springs, CO, USA, 20-22 March 1995 page 301 -page 304 — -/—	1,2,5,8, 12,13, 17,18,21

[X] Further documents are listed in the continuation of box C. [ ] Patent family members are listed in annex.

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 March 2000	31/03/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Szarowski, A

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Internatio application No
PCT/BE 99/00155

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	VIJAY D P ET AL: "ELECTRODES FOR PBZRXTI1-XO3 FERROELECTRIC THIN FILMS" JOURNAL OF THE ELECTROCHEMICAL SOCIETY,US,ELECTROCHEMICAL SOCIETY. MANCHESTER, NEW HAMPSHIRE, vol. 140, no. 9, 1 September 1993 (1993-09-01), pages 2640-2645, XP000424120 ISSN: 0013-4651 the whole document	1,2,5,8, 12,13, 17,18,21
A	NAKAMURA T ET AL: "ELECTRICAL PROPERTIES OF PZT THIN FILMS WITH IR AND IRO2 ELECTRODES" PROCEEDINGS OF THE IEEE INTERNATIONAL SYMPOSIUM ON APPLICATIONS OF FERROELECTRICS (ISAF),US,NEW YORK, IEEE, vol. SYMP. 9, 1995, pages 547-550, XP000764905 ISBN: 0-7803-1858-7 the whole document	1,2,5,8, 12,13, 17,18,21
A	TAKAGI T, OIZUKI I, KOBAYASHI I, OKADA M: "RuO2 Bottom Electrodes for Ferroelectric (Pb, La)(Zr, Ti)O3 Thin Films by Metalorganic Chemical Vapor Deposition" JAPANESE JOURNAL OF APPLIED PHYSICS, PART 1 (REGULAR PAPERS & SHORT NOTES), vol. 34, no. 8a, August 1995 (1995-08), pages 4104-4107, XP000885017 page 4104; figure 1	1,2,5, 12,17, 18,21
A	KUMAR A, ALAM M R: "Synthesis and characterization of ferroelectric thin films by KrF excimer laser ablation for memory applications" WARRENDALE, PA, USA, MATER. RES. SOC, USA, 1998, pages 211-217, XP000889711 Advances in laser ablation of materials. Symposium, San Francisco, CA, USA 13-16 April 1998 abstract; figure 2	1,2,6, 12,17, 18,22
A	YAMAMICHI S ET AL: "AN ECR MOCVD (BA,SR)TIO3 BASED STACKED CAPACITOR TECHNOLOGY WITH RUO2/RU/TIN/TISIX STORAGE NODES FOR GBIT-SCALE DRAMS" TECHNICAL DIGEST OF THE INTERNATIONAL ELECTRON DEVICES MEETING. (IEDM),US,NEW YORK, IEEE,1995, pages 119-122, XP000624707 ISBN: 0-7803-2701-2 figure 1	25

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INTERNATIONAL SEARCH REPORT

Internatio application No
PCT/BE 99/00155

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	NORGA G J, WOUTERS D J, BARTIC A, FE L, MAES H E: "Effect of Crystallisation on Fatigue in Sol-Gel PZT Ferroelectric Capacitors with Reactively Sputtered RuO2 Electrode Layers" PISCATAWAY, NJ, USA, IEEE, USA,1998, pages 3-6, XP000884492 ISAF 1998. Proceedings of the eleventh IEEE international symposium on applications of ferroelectrics, Montreux, Switzerland, 24-27 Aug. 1998 the whole document	

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